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Design of Phase-Locked Loop with Multiple Frequency Outputs for Communication Standards using VLSI Technology

[1]N. Shehanaz, Ph.D Scholar, APJ Abdul Kalam University, Indore

[2]Dr. Rahul Mishra, Associate Professor, APJ Abdul Kalam University, Indore.

Abstract-

Introducing a novel Phase-Locked Loop (PLL) design boasting multiple outputs, optimized for low power consumption and high speed, utilizing cutting-edge 45nm CMOS technology. This PLL operates within a broad frequency range, accepting input frequencies as low as 1MHz from external sources, while seamlessly generating multiple frequencies tailored for communication standards in high-speed Integrated Circuits (ICs), including protocols like Serial Peripheral Interface and Two-wire Interface .Crafted with meticulous attention to detail, this PLL design has undergone rigorous verification, including thorough parasitic extraction analysis. The outcome of this meticulous design approach is twofold: a significant reduction in power consumption and an expanded operational temperature range. These advancements promise enhanced efficiency and reliability, positioning this PLL as a cornerstone solution for next-generation communication systems demanding both performance and energy efficiency.

Keywords- CMOS (Complementary Metal Oxide Semiconductor), VCO (Voltage Controlled Oscillator), NB (Normal Distribution).

Introduction-

The Phase-Locked Loop (PLL) stands as a ubiquitous tool across diverse domains, including communication and instrumentation, where it finds utility in functions such as frequency synthesis and phase recovery, particularly within the microwave spectrum. Given the burgeoning demand for advancements in communication technology, significant endeavours have been directed towards the development of a proposed PLL leveraging VLSI

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technology. The choice of employing the 45-nanometer (nm) CMOS/VLSI technology warrants scrutiny. This selection stems from several key advancements associated with the 45 nm technology, notably the utilization of high-k gate oxide, metal gate materials, and extremely low-k interconnect dielectrics. In this technological paradigm, the effective gate length dwindles to a mere 25nm.

The 45 nm technology harbours distinctive attributes pivotal to its appeal, including heightened performance, enhanced integration density, and minimized power consumption. These features collectively underpin its suitability for accommodating the intricacies of modern communication systems, thereby justifying its adoption in the design of the proposed PLL.in table 1.1 below.

S.No.	Parameter	Value
1	VDD (V)	0.85-1.2 V
2	I_{off} N (nA/um)	5-100
3	I_{off} P (nA/um)	5-100
4	Gate dielectric	SiON, HfO_2
5	No. of metal layers	6-10

Table 1 Specifications of 45 nm technologies for PLL

Design of PLL Using 45 nm Technology-

Since the multiple outputs Phase Locked Loop (PLL) provides multiple clock generation, it is to be needed to design PLL with multiple output for modern communication Engineering applications with low power, high stability and low jitter. A lot of work has been taken in the PLL design, for different applications, using VLSI/CMOS technology. Since the multiple outputs PLL provides multiple clock generation in radar applications & multichannel communication, it is research problem to design PLL with multiple output for

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modern communication engineering applications with low power, high stability and high frequency.

For low power, low leakage transistors are used and will compromise on little frequency. Also there will be a shutdown input in proposed circuit which will bring the PLL to hold or there can be a pin, which if enabled then will make the PLL frequency to half.

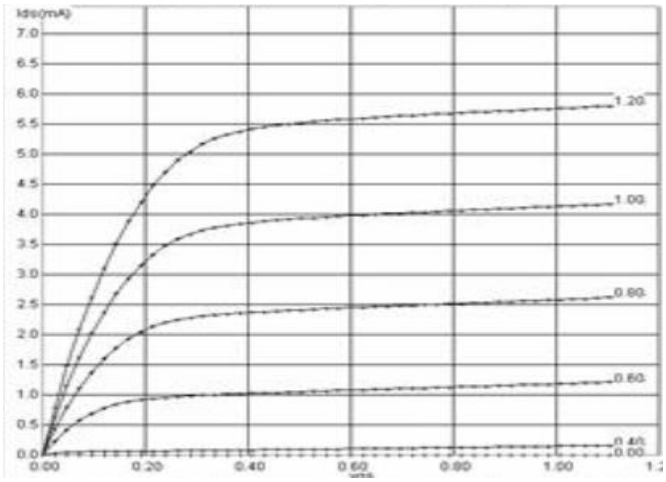

Fig 1 Implementation of BSIM4 within MICROWIND3.1

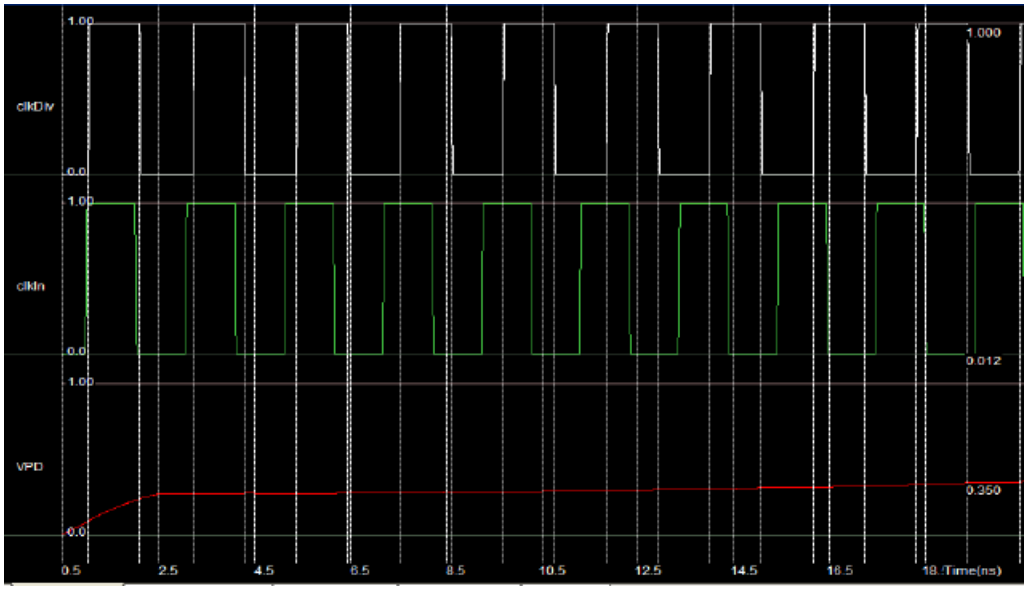

Fig 2 voltage verses time response of phase detector

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Sr. No.	Vdd(V)	freq(GHz)
1	0.80	6.211
2	1.00	6.211
3	1.20	7.770
4	1.40	9.116

Table 2 Voltage variation of V_{DD} verses frequency of node V_{high}

Design of VCO Using 45 nm Technology-

The layout of VCO which is develop by us is a modified design of high performance VCO.This is a optimum design for use in industries at 45 nm VLSI technology. In the estimated design more emphases is given on power consumption, layout design and many more.

Oscillators are required to generate the carrying signals for radio frequency transmission, but also for the main clocks of processors. The high performance VCO provides very good linearity as compared to previous one. In Microwind, the threshold and mobility parameters are varying with a normal distribution <Gloss>, with a typical variation of 10%.

The delay dependence on $V_{control}$ is almost linear for the fall edge. The key point is to design an inverter just after the delay-cell with a very low commutation point Vc. The rise edge is almost unchanged.

Result Analysis of PLL-

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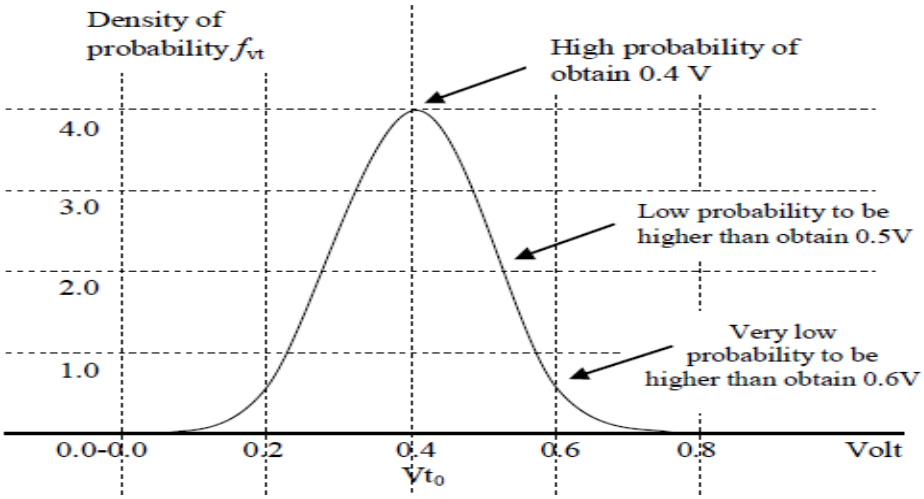

Fig 3 The NB of Vt, with a typical variation of 10%

Since the PLL, provide multiple clock generation, it is a research problem to design PLL using 45nm process technology parameters which will offers high speed performance at low power. Optimum layout for 3.45 GHz PLL is designed using high performance VCO, which is almost stable when Vc reaches to 0.501 volt. From the parametric analysis of design tool shown in fig 9.5, it is observed that the power dissipation measured by VDD at 1Volt is found 0.113miliwatt, which shows that power consumption is very low.

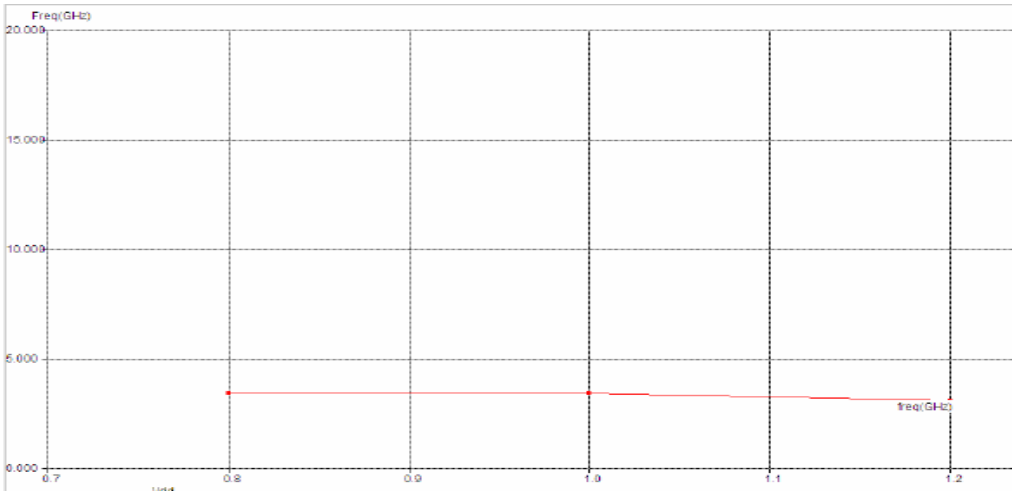

Fig 4 Voltage variation of vdd verses frequency of node Vhigh

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Due to advancements in technology scaling, there's been a rise in process variations affecting key circuit parameters like transistor channel length and threshold voltage. These variations exert a notable influence on circuit performance and can also shape the design considerations for parallel systems. The layout design in question leverages 29 NMOS and 28 PMOS BSIM4 transistors, each meticulously dimensioned alongside optimal metal connections adhering to lambda-based rules of microwind. This approach ensures robustness against process variations, enhancing the reliability and stability of the implemented design microwind 3.1 software.

Conclusion:-

In CMOS digital integrated circuits, the level of power dissipation during switching is closely tied to the power supply voltage, making the reduction of VDD a potent strategy for curbing overall power consumption. In the envisioned PLL design, a power supply voltage (VDD) of 1 volt has been adopted. The illustration depicts the pinnacle of efficiency: a meticulously crafted chip design for a low-power PLL, engineered to deliver multiple (four) outputs, harnessing the capabilities of 45nm VLSI technology. This optimized design represents a synthesis of efficiency and performance, poised to meet the demands of contemporary applications while minimizing energy consumption.

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